PVP 14

Code: IT3T1

II B.Tech - I Semester–Regular/Supplementary Examinations
November 2016

DIGITAL SYSTEM DESIGN
(INFORMATION TECHNOLOGY)

Duration: 3 hours Max. Marks: 70

PART – A

Answer ***all*** the questions. All questions carry equal marks

11x 2 = 22 M

1.

a) Convert the hexadecimal number 68BE to binary and octal.
b) Find the hex sum of $(93)_{16}$ + $(DE)_{16}$.
c) Draw symbol and construct the truth table for NAND gate.
d) Arrange the following as per their operator precedence. NOT, OR, AND, parenthesis.
e) Write the dual of x'yz' + x'y'z.
f) Define multiplexer.
g) Define encoder.
h) Define programmable array logic.
i) Draw the block diagram of memory unit.
j) Draw the logic diagram and characteristic equation of RS flip-flop.
k) Draw the 4-bit binary ripple counter.

PART – B

Answer any ***THREE*** questions. All questions carry equal marks.

3 x 16 = 48 M

2.

a) Convert the following into Octal. 6 M

i) $(0.503)_{10}$ ii) $(1010101)_{2}$ iii) $(ABCD)_{16}$

b) Represent the decimal number 5,6 in binary form using

i) BCD code ii) Excess-3 code

iii) Gray code iv) 8421 code 10 M

3.

a) Find the complement of the following expressions:

i) (x+y'+z)(x'+z')(x+y) ii) (AB'+C)D'+E

iii) xy'+x'y. 6 M

b) Simplify the following Boolean function, using three-variable K-map: 10 M

i) F(x,y,z)=∑(0,1,5,7) ii)F(x,y,z)= ∑(1,2,3,6,7)

4.

a) Explain about the following with logic diagram and truth table. i) Half Adder ii) Full Adder 8 M

b) Draw the diagram of 4-bit adder and explain its working procedure. 8 M

5.

a) Explain PLA with necessary diagrams. 10 M

b) Compare PROM, PLA and PAL. 6 M

6.

a) Explain JK Flip-flop. What is the disadvantage of it and how it can be eliminated? 8 M

b) Draw and explain 4-bit universal shift register. 8 M